REMARKS

In response to the Office Action mailed April 18, 2002, the Applicants respectfully request reconsideration.

Claims 1-18, which were previously examined, are pending for examination, of which claims 1, 7, 19 and 20 are independent. Applicant notes with appreciation the allowance of claims 19 and 20.

1. Summary of Telephone Interviews

Applicant and Applicant's representatives appreciate the courtesies extended by Examiner Nadav in granting and conducting telephone interviews on March 9, 2004 with Applicant's representatives Daniel P. McLoughlin and James H. Morris, and on March 15, 2004, with Daniel P. McLoughlin. The substance of these interviews is fully summarized below.

During the telephone interviews, the rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,382,837 (Aiello) was discussed. Specifically, Applicant sought clarification regarding the Office Action's assertion (section 2, page 3, lines 8-11) that Aiello teaches "a second bipolar transistor... for coupling the isolation region to the substrate... when the substrate potential is lower than the reference potential and the first bipolar transistor is off," as recited in claim 1. Examiner Nadav explained that his position is based on the fact that any reference potential disclosed in Aiello could serve as a teaching of the reference potential recited in claim 1 because the reference potential in claim 1 is not limited to any particular value. Applicant's representative agreed that the reference potential recited in claim 1 is not limited to any particular value, but stressed that for Aiello to anticipate claim 1, Aiello must teach, among other things, a reference potential that meets every limitation of the reference potential recited in claim 1.

Examiner Nadav suggested that Applicant respond in writing to the Final Office Action to further clarify Applicant's position, so that he will have the opportunity to more carefully consider the teachings of Aiello with respect to claim 1. Accordingly, Applicant hereby submits this Request for Reconsideration.

2. The Drawings Satisfy the Requirements of 37C.F.R. § 1.83(a)

The drawings stand rejected (Section 1) under 37 C.F.R. § 1.83(a) because the "emitter of the first bipolar transistor being directly connected to the isolation region, as recited in claims 12 and 17, must be shown in Fig. 7." Applicant respectfully traverses this rejection.

37 C.F.R. § 1.83(a) requires that the drawings show each feature specified in the claims. Fig. 5 illustrates an example of a bipolar transistor, Q33, having an emitter directly connected to an isolation region, ISO. Accordingly, the drawings already show an emitter of a first bipolar transistor being directly connected to an isolation region, as recited in claims 12 and 17. Thus, there is no need to amend Fig. 7 as suggested by the Office Action.

In view of the foregoing, the drawings satisfy the requirements of 37 C.F.R. § 1.83(a). Accordingly, Applicant respectfully requests that the objection to the drawings under 37 C.F.R. § 1.83(a) be withdrawn.

3. Claims 1-6 and 10-14 Patentably Distinguish Over Aiello

Claims 1-6, 10, 11, 13 and 14 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over U.S. Patent No. 5,382,837 (Aiello). Applicant respectfully traverses this rejection.

3.1 Discussion of Aiello

Aiello is directed to a switching circuit that connects a first circuit node to either a second or a third circuit node relative to a voltage potential on the third circuit node, and that controls the potential of an insulation region of an integrated circuit in relation to the potential of the substrate. (Col. 1, lines 7-12).

Aiello illustrates several embodiments of the switching circuit (Figs. 1-6). Each embodiment includes a transistor T1 having an emitter connected to a ground potential, a collector connected to a an insulation region (Viso) and a base coupled to a power supply Vcc through a resistor R1. Each embodiment further includes a transistor T2 (a first bipolar transistor according to the Final Office Action, page 3, line 3) having an emitter connected to a substrate (Vsub) and a collector connected to Viso. (Figs. 1-6; Col. 3, line 37-col. 6, line 38). Some embodiments (Figs. 3-6) include a transistor T4 having an emitter connected to the base of T2,

and some embodiments (Figs. 2, 4 and 6) include a transistor T3 having an emitter connected to Vsub, a collector coupled to Vcc through a resistor R1 and a base connected to the base of T2.

Aiello indicates that, when the potential of the substrate is greater than a reference potential (e.g., Vsub > zero), T2 is off and T1 is in saturation mode, thereby coupling the insulation region to the ground voltage. (Col. 3, line 59-col. 4, line 3; col. 4, lines 34-46).

Contrary to the assertions of the Final Office Action (Section 2, page 3, lines 7-11), Aiello does *not* disclose that the transistor T3 (Figs. 2, 4 and 6) couples the insulation region (Viso) to the substrate (Vsub) when the substrate potential is greater than the reference potential *and T2 is off*. Rather, Aiello discloses that **when the substrate potential is less than a reference potential** (e.g., Vsub<zero), **T2 is in saturation mode.** (Col. 4, lines 4-24, 47-54; Col.6, lines 14-17; emphasis added).

3.2 Claim 1 is Not Rendered Obvious by Aiello

The Office Action asserts that it would have been obvious to a person of ordinary skill in the art to use Aiello's switching circuit as a protection structure against polarity inversion of a substrate potential. Applicant agrees, as Applicant describes, in the specification (page 3, lines 6-19), using Aiello's switching circuit as a protection structure.

Claim 1 patentably distinguishes over Aiello because Aiello fails to teach or suggest an integrated circuit including, *inter alia*, a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for **coupling the isolation region to the substrate** through a high-impedance **when the substrate potential is lower than the reference potential and the first bipolar transistor is off**, as recited in claim 1. Rather, Aiello teaches that, when a substrate potential is lower than the reference potential, the first bipolar transistor (T2) is *not* off, but is operating *in saturation mode*.

In view of the foregoing, claim 1 is not rendered obvious by Aiello. Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Aiello be withdrawn.

Claim 2-6 and 10-14 each depend directly or indirectly from claim 1 and are patentable over Aiello for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of claims 2-6, 10, 11, 13 and 14 under §103(a) be withdrawn.

4. Claims 7-9 and 15-18 Patentably Distinguish Over Aiello

Claims 7-9, 15, 16 and 18 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over U.S. Patent No. 5,382,837 (Aiello et al.) Applicant respectfully traverses this rejection because Aiello fails to teach or suggest all of the limitation of claim 7. Specifically, Aiello fails to teach or suggest a semiconductor device, comprising: a vertical power component having a terminal formed by a substrate of a first conductivity type; a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and a protection structure against polarity inversion of a substrate potential, comprising: a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit; a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and **means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential *and the first bipolar transistor is off***, as recited in claim 7.

Therefore, for at least these reasons, claim 7 is not rendered obvious by Aiello. Accordingly, Applicant respectfully requests that the rejection of claim 7 under 35 U.S.C. §103(a) as being unpatentable over Aiello be withdrawn.

Claims 8, 9 and 15-18 each depend directly or indirectly from claim 7 and are patentable over Aiello for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of claims 8, 9, 15, 16 and 18 under §103(a) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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